WHAT IS CLAIMED IS:

1. A method of exporting emulation information from a data processor, comprising:

collecting internal emulation information within a data processor;

arranging the collected emulation information into a plurality of first information blocks;

receiving the plurality of first information blocks and arranging the emulation information contained therein into a plurality of second information blocks which differ in size from the first information blocks; and

outputting a sequence of the second information blocks from the data processor via a plurality of terminals of the data processor.

2. The method of Claim 1, wherein the second information blocks are smaller in size than the first information blocks.

3. The method of Claim 1, including receiving the sequence of second information blocks externally of the data processor, and re-arranging the emulation information contained in the second information blocks into a plurality of the first information blocks.

4. The method of Claim 1, wherein each of the first and second information blocks is a packet of emulation information.

5. The method of Claim 1, wherein said last-mentioned arranging step includes forming one of the second information blocks solely from a portion of one of the first information blocks.

6. The method of Claim 5, wherein said last-mentioned arranging step includes forming each of the second information blocks solely from a portion of one of the first information blocks.

7. The method of Claim 5, wherein said outputting step includes outputting the sequence of second information blocks at a higher block rate than a block rate at which said sequence of first information blocks is received.

8. The method of Claim 1, wherein said last-mentioned arranging step includes combining in one of said second information blocks emulation information from more than one of said first information blocks.

9. The method of Claim 8, wherein said last-mentioned arranging step includes combining in each of said second information blocks emulation information from more than one of said first information blocks.

10. The method of Claim 8, wherein said outputting step includes outputting the sequence of second information blocks at a lower block rate than a block rate at which said sequence of first information blocks is received.

11. The method of Claim 8, wherein said receiving step includes receiving said first information blocks in a sequence, said combining step including combining in

said one second information block emulation information from consecutive ones of said first information blocks in the sequence of first information blocks.

12. The method of Claim 11, wherein said combining step includes combining in each of said second information blocks information from consecutive ones of said first information blocks in the sequence of first information blocks.

13. The method of Claim 11, wherein said outputting step includes outputting the sequence of second information blocks at a lower block rate than a block rate at which said sequence of first information blocks is received.

14. The method of Claim 8, wherein the second information blocks are larger in size than the first information blocks.

15. The method of Claim 1, wherein said outputting step includes inserting a NOP block into the sequence of second information blocks.

16. An integrated circuit, comprising:

a data processor for performing data processing operations;

a collector coupled to said data processor for collecting emulation information from said data processor and arranging said emulation information into a plurality of first information blocks;

an exporter coupled to said collector for receiving therefrom said plurality of first information blocks and arranging said emulation information contained therein into a

plurality of second information blocks which differ in size from said first information blocks;

a plurality of terminals for outputting information; and

said exporter coupled to said terminals for outputting a sequence of the second information blocks via said terminals.

17. The integrated circuit of Claim 16, wherein said second information blocks are smaller in size than said first information blocks.

18. The integrated circuit of Claim 16, wherein said exporter is operable for forming one of said second information blocks solely from a portion of one of said first information blocks.

19. The integrated circuit of Claim 18, wherein said exporter is operable for outputting said sequence of second information blocks at a higher block rate than a block rate at which said exporter has received said sequence of first information blocks.

20. The integrated circuit of Claim 16, wherein said exporter includes a combiner for combining in one of said second information blocks emulation information from more than one of said first information blocks.

21. The integrated circuit of Claim 20, wherein said exporter is operable for outputting said sequence of second information blocks at a lower block rate than a block rate at which said exporter has received said sequence of first information blocks.

22. The integrated circuit of Claim 20, wherein said second information blocks are larger in size than said first information blocks.

23. The integrated circuit of Claim 20, wherein said collector is operable for providing said first information blocks to said exporter in a sequence, said combiner operable for combining in said one second information block emulation information from consecutive ones of said first information blocks in said sequence of first information blocks.

24. The integrated circuit of Claim 23, wherein said exporter is operable for outputting said sequence of second information blocks at a lower block rate than a block rate at which said exporter has received said sequence of first information blocks.

25. The integrated circuit of Claim 23, wherein said exporter includes a storage apparatus for storing therein consecutive ones of said first information blocks, said combiner coupled to said storage apparatus.

26. The integrated circuit of Claim 23, wherein said second information blocks are larger in size than said first information blocks.

27. A data processing system, comprising:

an integrated circuit, including a data processor for performing data processing operations;

an emulation controller coupled to said integrated circuit for controlling emulation operations of said data processor;

said integrated circuit including an apparatus coupled between said data processor and said emulation controller for providing emulation information about said data processing operations, said apparatus including a collector coupled to said data processor for collecting said emulation information from said data processor and arranging said emulation information into a plurality of first information blocks, and an exporter coupled to said collector for receiving plurality of first information blocks and arranging said emulation information contained therein into a plurality of second information blocks which differ in size from said first information blocks; and

said integrated circuit including a plurality of terminals coupled to said emulation controller for outputting information to said emulation controller, said exporter coupled to said terminals for outputting a sequence of said second information blocks to said emulation controller via said terminals.

28. The system of Claim 27, including a man/machine interface coupled to said emulation controller for permitting a user to communicate with said emulation controller.

29. The system of Claim 28, wherein said man/machine interface includes one of a visual interface and a tactile interface.